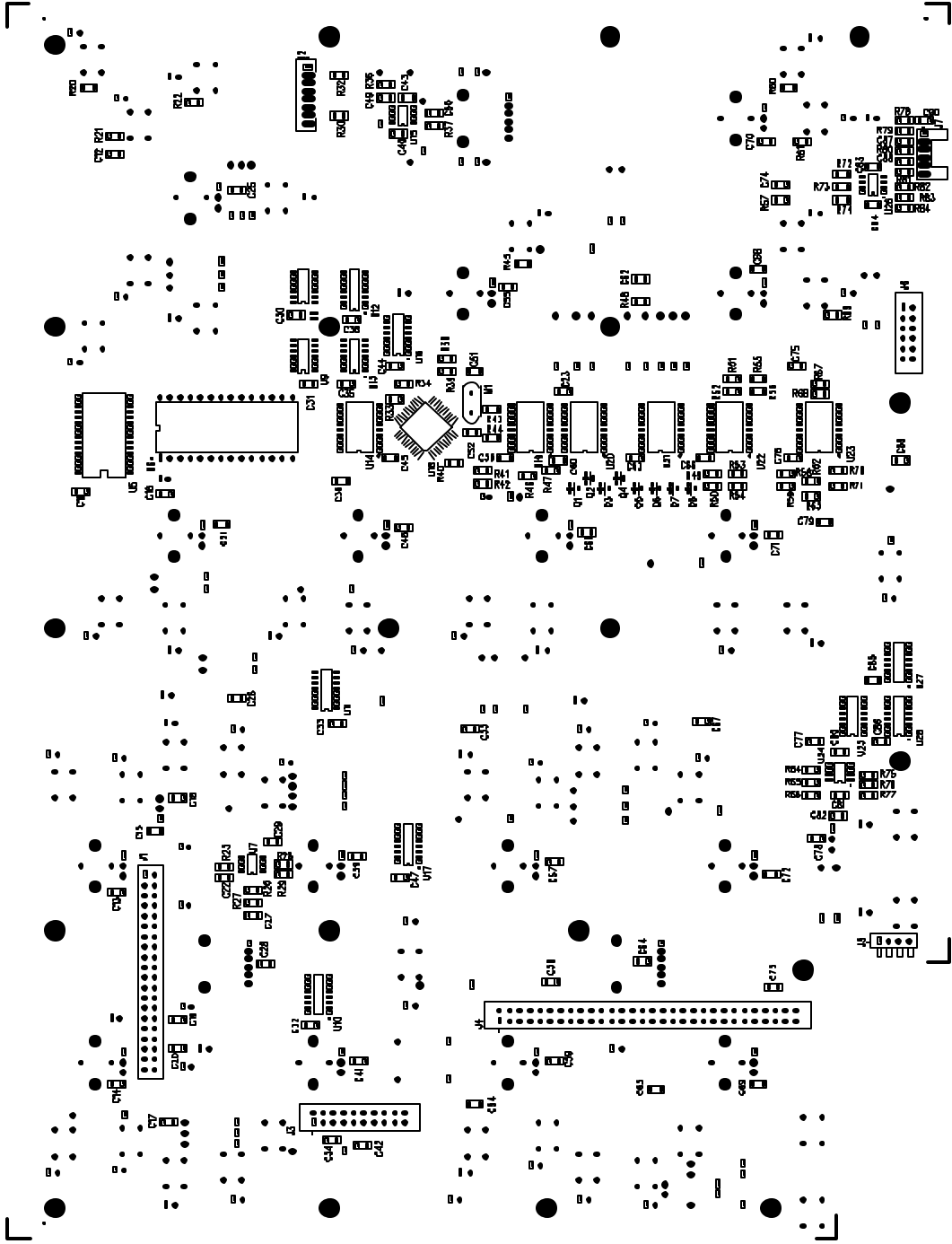
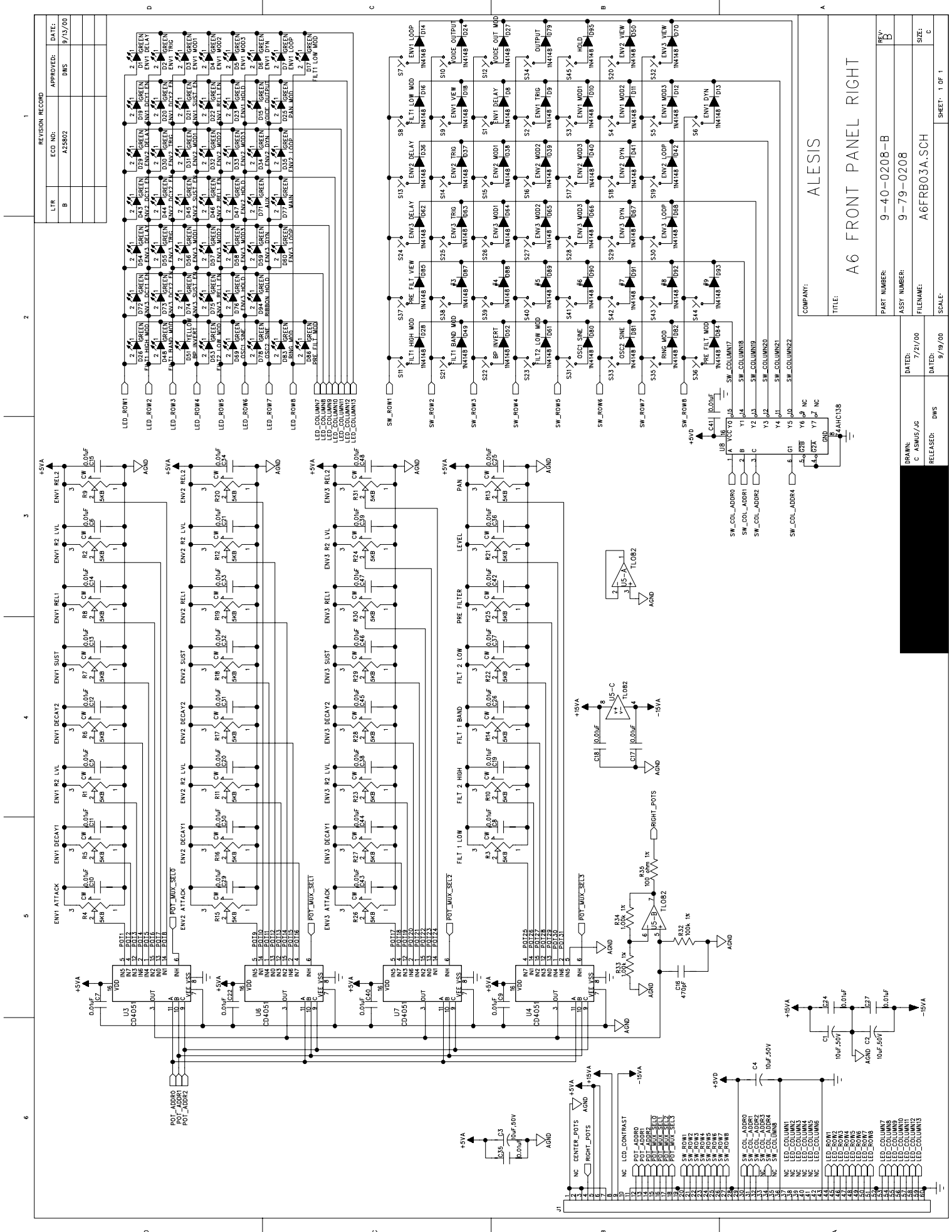


ALESIS BOTTOM ASSEMBLY DRAWING 9-79-0206-C



1. Mount the following parts on the backside of the PCB and head holder of the Uplink. Insert J1-7 (1-1000), J1-8 (1-1000), J1-9 (1-1000), J1-10 (1-1000), J1-11 (1-1000), J1-12 (1-1000), J1-13 (1-1000), J1-14 (1-1000), J1-15 (1-1000), J1-16 (1-1000), J1-17 (1-1000), J1-18 (1-1000), J1-19 (1-1000), J1-20 (1-1000), J1-21 (1-1000), J1-22 (1-1000), J1-23 (1-1000), J1-24 (1-1000), J1-25 (1-1000), J1-26 (1-1000), J1-27 (1-1000), J1-28 (1-1000), J1-29 (1-1000), J1-30 (1-1000), J1-31 (1-1000), J1-32 (1-1000), J1-33 (1-1000), J1-34 (1-1000), J1-35 (1-1000), J1-36 (1-1000), J1-37 (1-1000), J1-38 (1-1000), J1-39 (1-1000), J1-40 (1-1000), J1-41 (1-1000), J1-42 (1-1000), J1-43 (1-1000), J1-44 (1-1000), J1-45 (1-1000), J1-46 (1-1000), J1-47 (1-1000), J1-48 (1-1000), J1-49 (1-1000), J1-50 (1-1000), J1-51 (1-1000), J1-52 (1-1000), J1-53 (1-1000), J1-54 (1-1000), J1-55 (1-1000), J1-56 (1-1000), J1-57 (1-1000), J1-58 (1-1000), J1-59 (1-1000), J1-60 (1-1000), J1-61 (1-1000), J1-62 (1-1000), J1-63 (1-1000), J1-64 (1-1000), J1-65 (1-1000), J1-66 (1-1000), J1-67 (1-1000), J1-68 (1-1000), J1-69 (1-1000), J1-70 (1-1000), J1-71 (1-1000), J1-72 (1-1000), J1-73 (1-1000), J1-74 (1-1000), J1-75 (1-1000), J1-76 (1-1000), J1-77 (1-1000), J1-78 (1-1000), J1-79 (1-1000), J1-80 (1-1000), J1-81 (1-1000), J1-82 (1-1000), J1-83 (1-1000), J1-84 (1-1000), J1-85 (1-1000), J1-86 (1-1000), J1-87 (1-1000), J1-88 (1-1000), J1-89 (1-1000), J1-90 (1-1000), J1-91 (1-1000), J1-92 (1-1000), J1-93 (1-1000), J1-94 (1-1000), J1-95 (1-1000), J1-96 (1-1000), J1-97 (1-1000), J1-98 (1-1000), J1-99 (1-1000), J1-100 (1-1000).
2. Right angle header J1-1 (1-1000) should be mounted with pins pointing towards board edge.



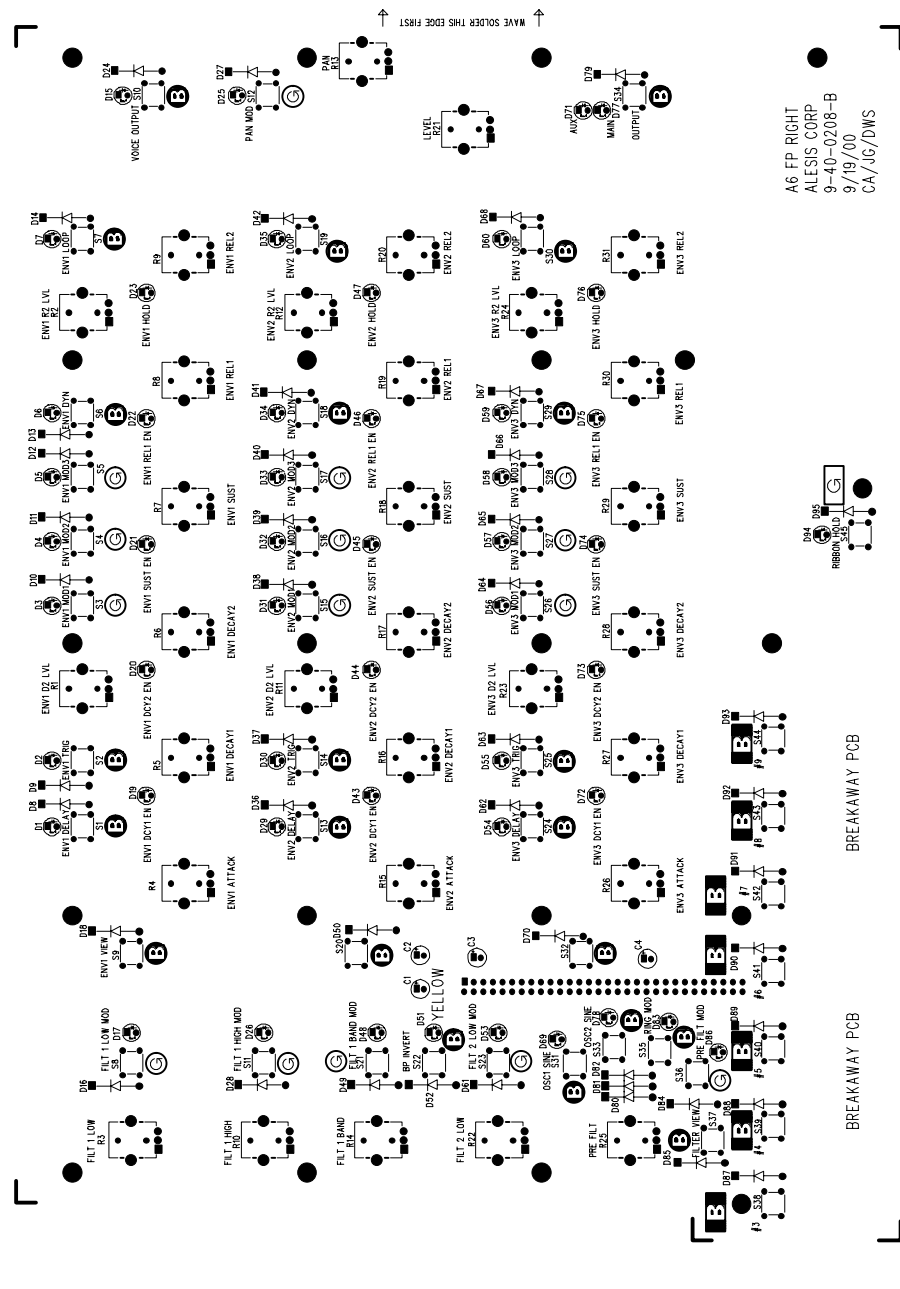
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:
B	A23802	DWS	9/13/00

COMPANY:		ALESYS	
TITLE:		A6 FRONT PANEL RIGHT	
PART NUMBER:	9-40-0208-B	REV:	B
ASSY NUMBER:	9-79-0208	SIZE:	C
FILENAME:	A6FRB03A.SCH		
SCALE:			

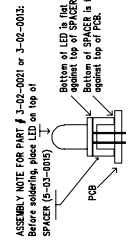
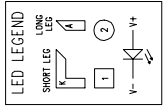
DRAWN:	C. ASHES/GG	DATED:	7/21/00
RELEASED:	DWS	DATED:	9/19/00

SCALE:	1 OF 1
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ALESIS ASSEMBLY DRAWING 9-79-0208-B



A6, FP RIGHT
 ALESIS CORP
 9-40-0208-B
 9/19/00
 CA/JG/DWS

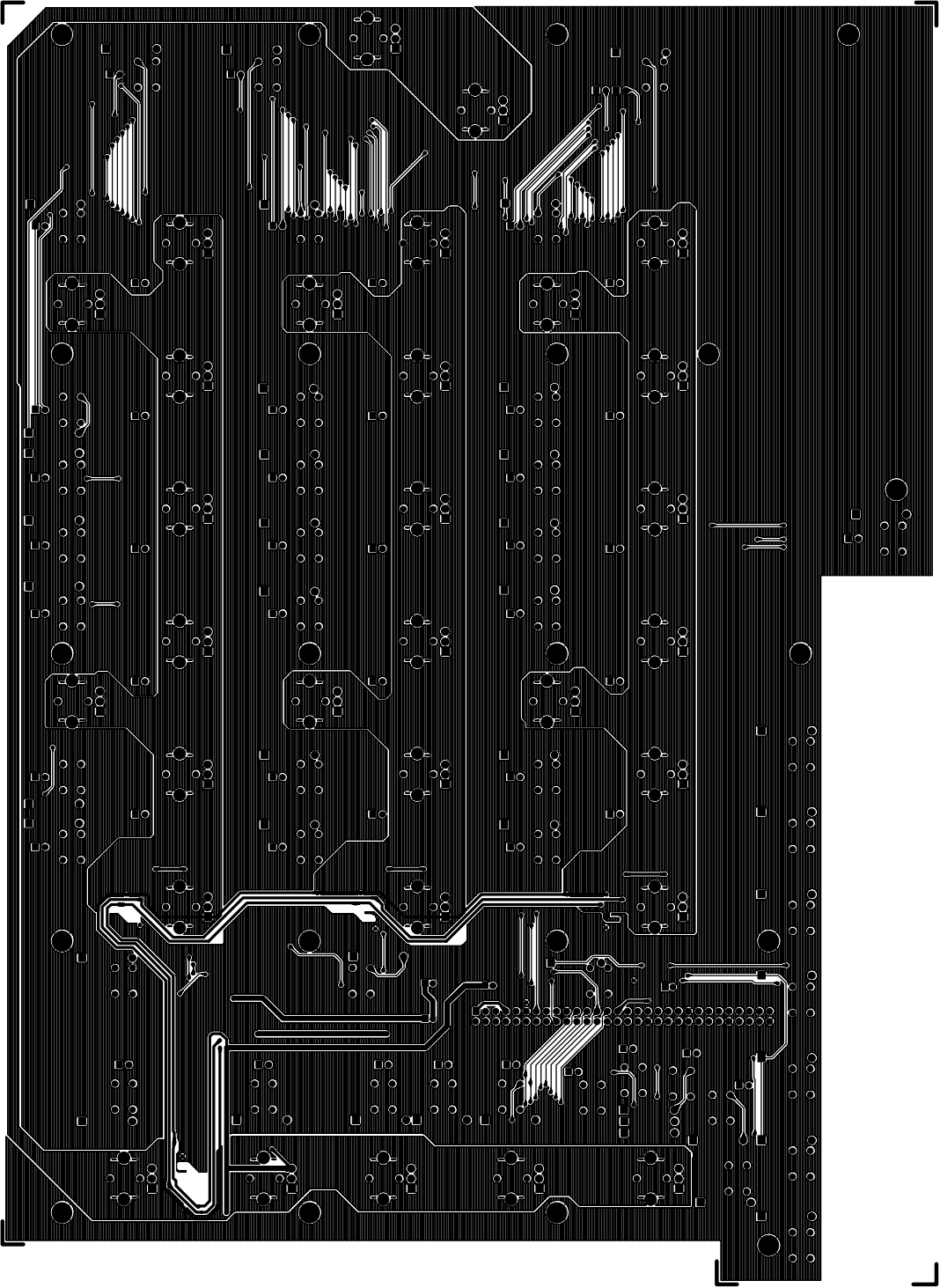


1. Hand stuff all thru-hole components (except J1) on the TOP SIDE.
2. Insert J1 (60-pin DIL header) on BOTTOM SIDE and handsolder. (Mask pads of J1 before waversoldering surface mount components on bottom side).
3. Refer to drawings (see below) for assembling and inserting LEDs and spacers. Insert spacers with LED flush against PCB. D51 is a yellow LED (3-02-0013) and is marked "YELLOW". All other LEDs are green (3-02-0021) and are unmarked.
4. Detach BREAKAWAY PCB after wave-soldering.
5. VERY IMPORTANT: ALL POTS (0-09-1096) SWITCHES (6-02-0050) AND LED ASSEMBLIES (SEE BELOW) MUST BE PERFECTLY FLUSH (FLAT) AGAINST THE PCB
6. Board to be wave soldered using Alesis supplied solder fixture.
7. Wave solder all surface mount parts and thru hole leads.
8. Board designed to be wave soldered, straight edge first (refer to notes on top assembly drawing)
9. SWITCHCAP LEGEND: "B" in a circle for BLACK circular switchcaps "G" in a circle for GRAY circular switchcaps. "B" in a rectangle for BLACK rectangular switchcaps. "G" in a rectangle for GRAY rectangular switchcaps.

ALESIS 9-40-0208-B "TOPSILK"

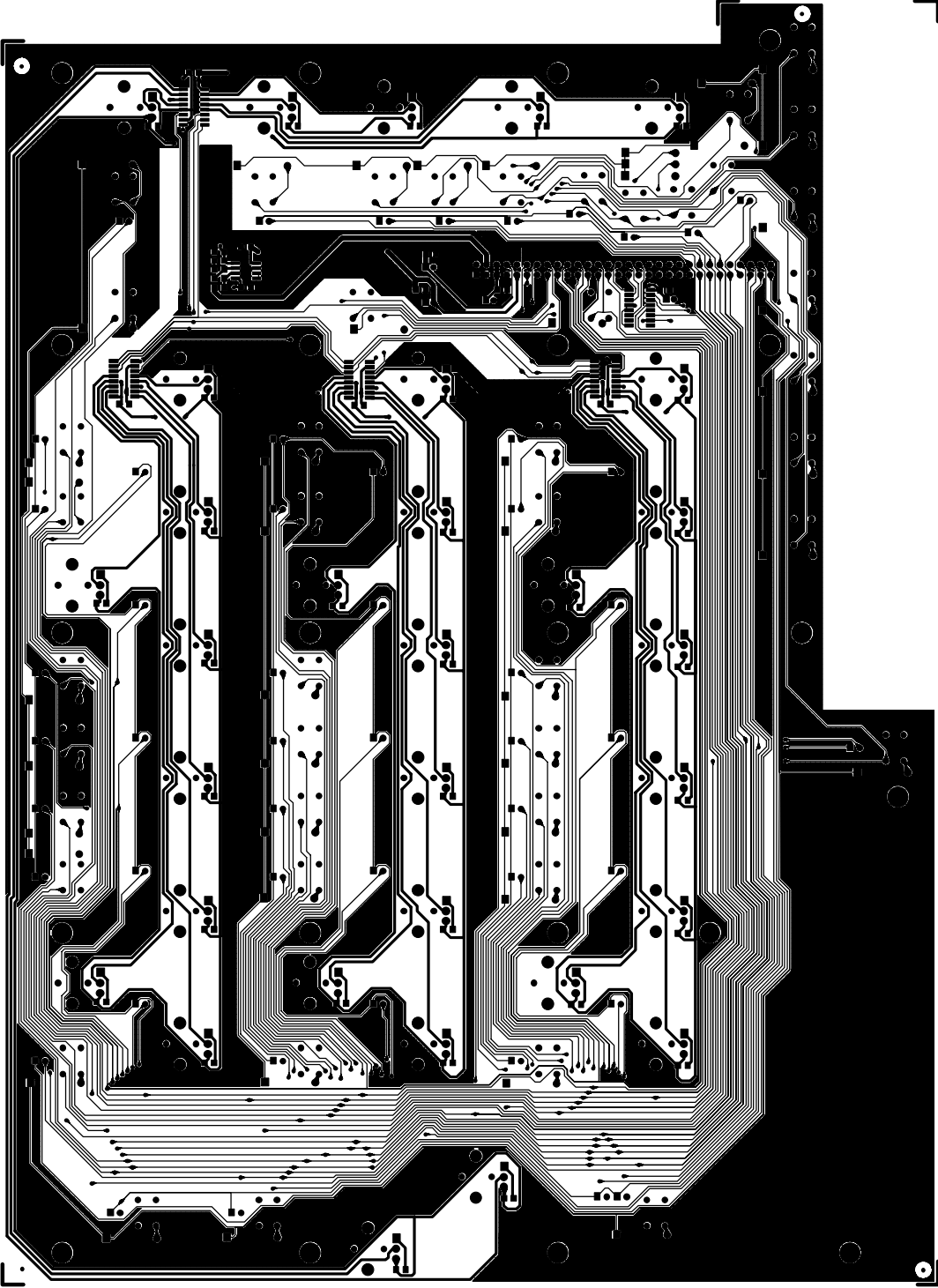
BREAKAWAY PCB

BREAKAWAY PCB



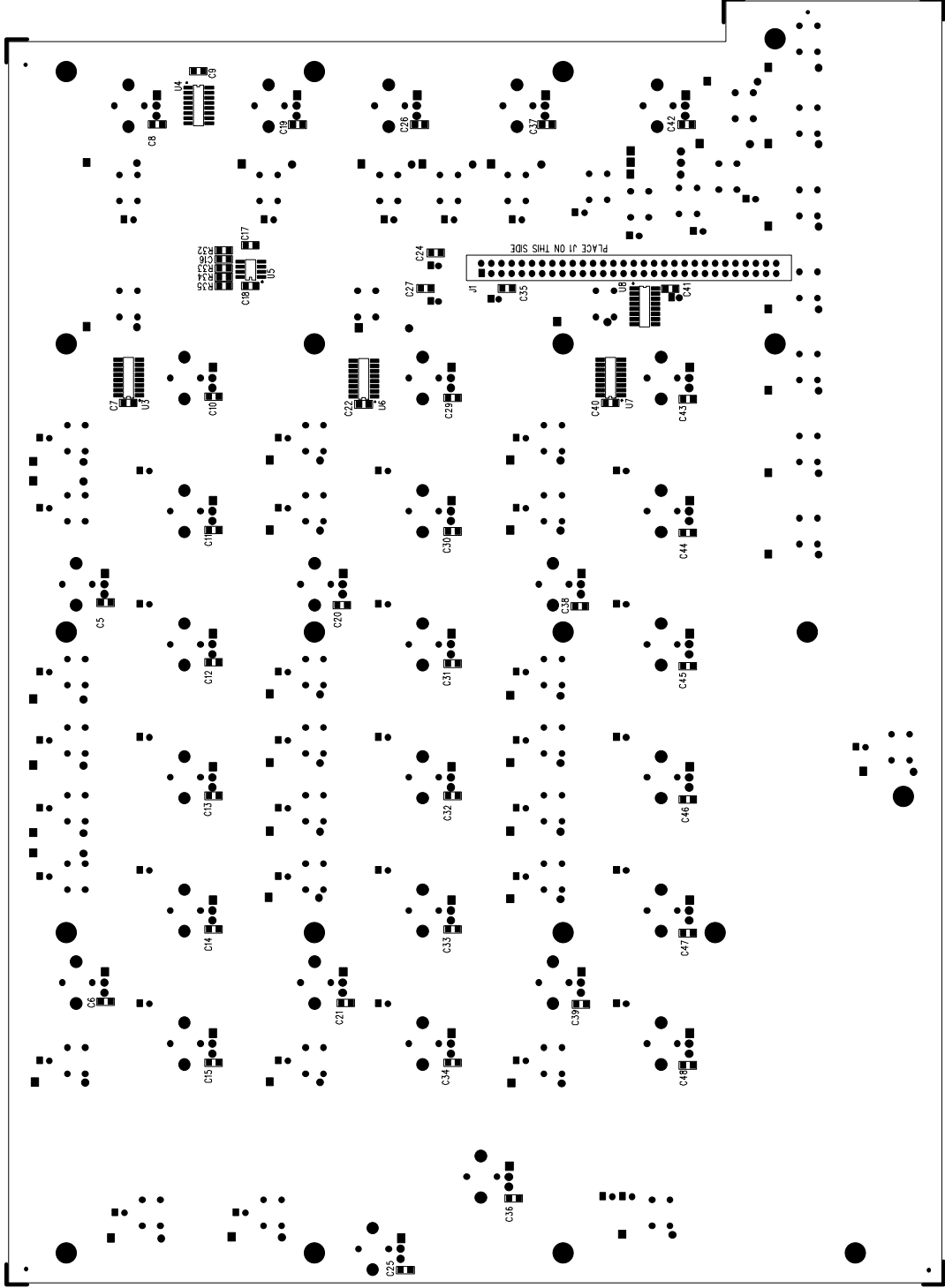
ALESIS 9-40-0208-B "TOP TRACE"



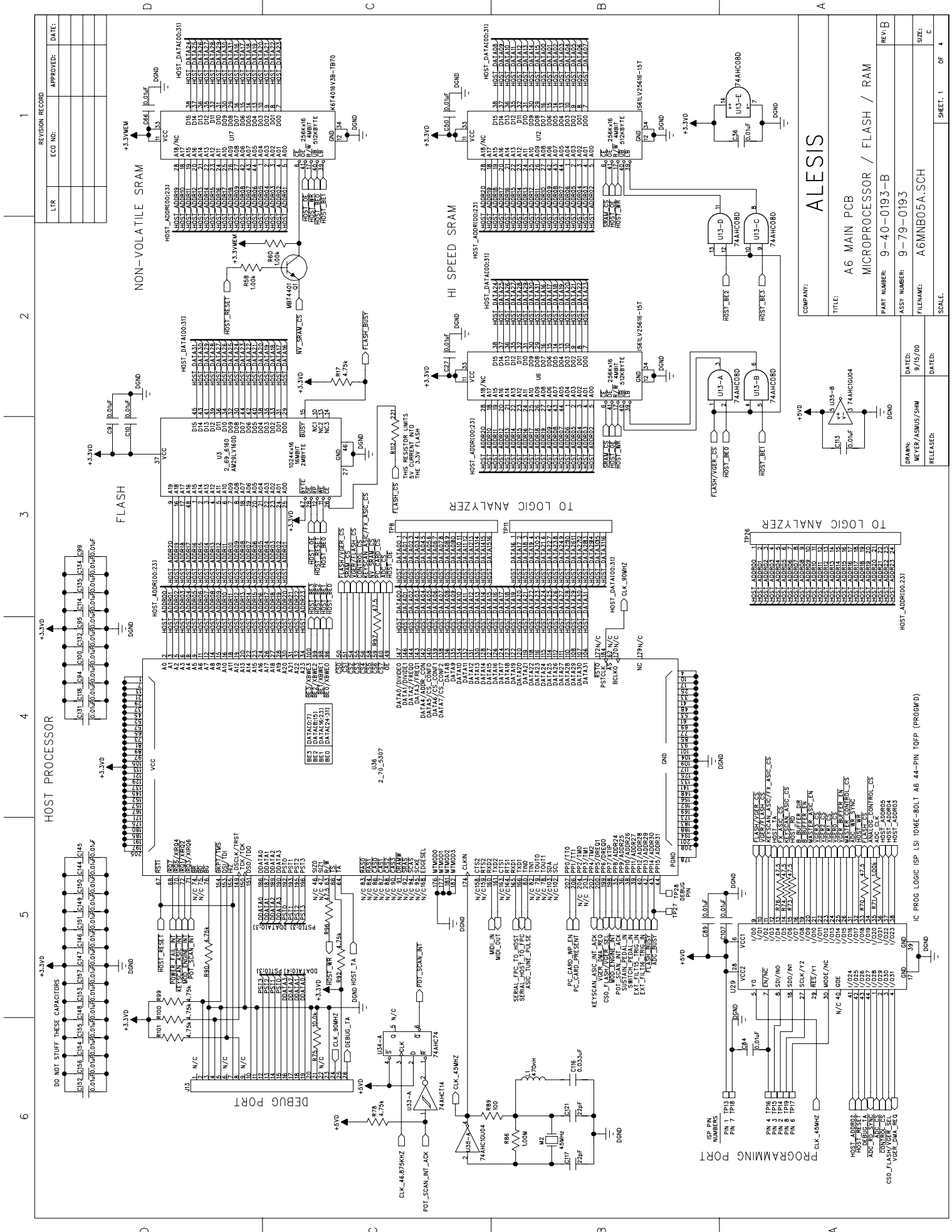


ALESIS 9-40-0208-B "BOTTRACE"

ALESIS 9-40-0208-B "BOTASSY"



2. Insert J1 (60-pin DIL header) on BOTTOM SIDE and handsolder. (Mask pads of J1 before wavesoldering surface mount components on bottom side).

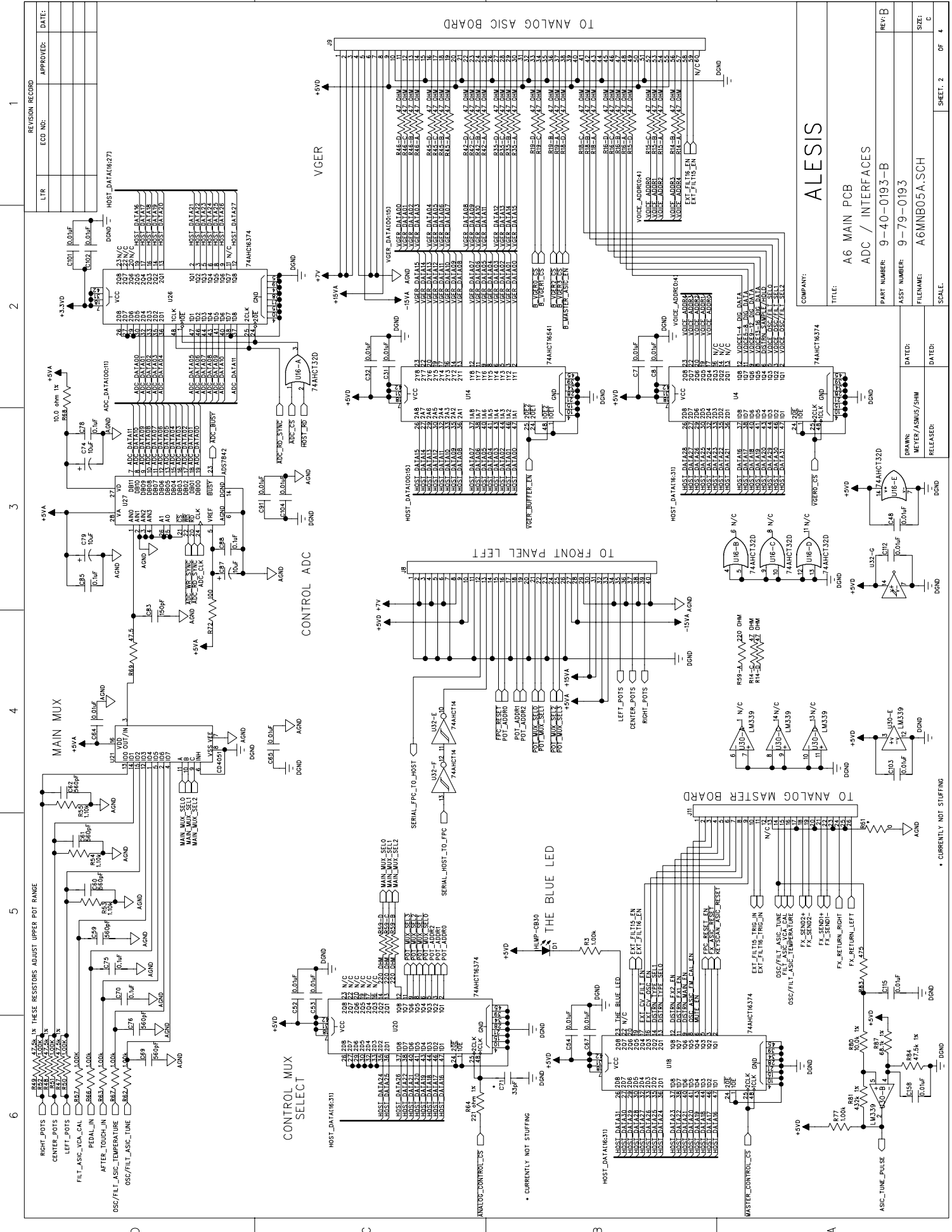


REVISION RECORD		APPROVED:	DATE:
LTR	ECD		

COMPANY:	ALESIS		
TITLE:	A6 MAIN PCB		
PART NUMBER:	9-40-0193-B		
ASSY NUMBER:	9-79-0193		
FILENAME:	AGMNB05A.SCH		
SCALE:	SHEET 1 OF 4		

FRMWR:	MEYER/ASMS/SHM	DATE:	9/15/00
RELEASED:		DATE:	

IC PROG LOGIC (SP LSI 1018E-80LT A6 44-PIN TQFP (PROGWD))	
---	--



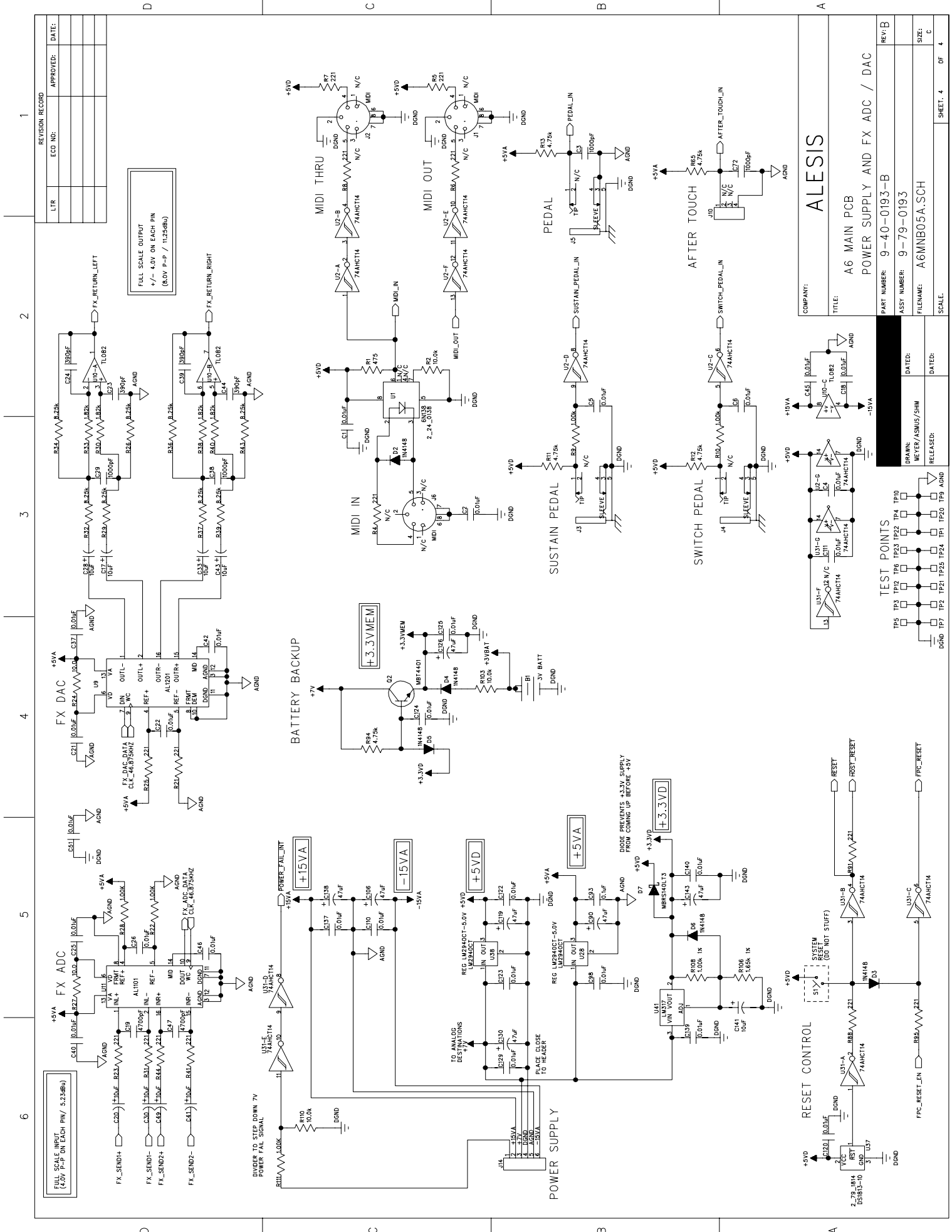
ALESIS

COMPANY: A6 MAIN PCB
 TITLE: ADC / INTERFACES
 PART NUMBER: 9-40-0193-B
 ASSY NUMBER: 9-79-0193
 FILENAME: AGMNB05A.SCH
 SCALE: 1:1

DATE: _____
 DATED: _____
 DATE: _____
 DATED: _____
 DRAWN: MFER/ASMUS/SHM
 RELEASED: _____

REV: B
 SIZE: C
 SHEET: 2 OF 4

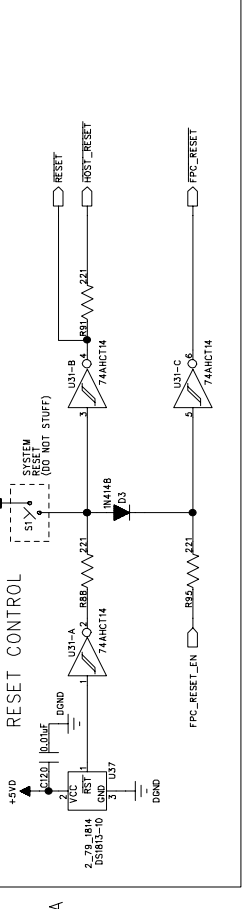
* CURRENTLY NOT STUFFING



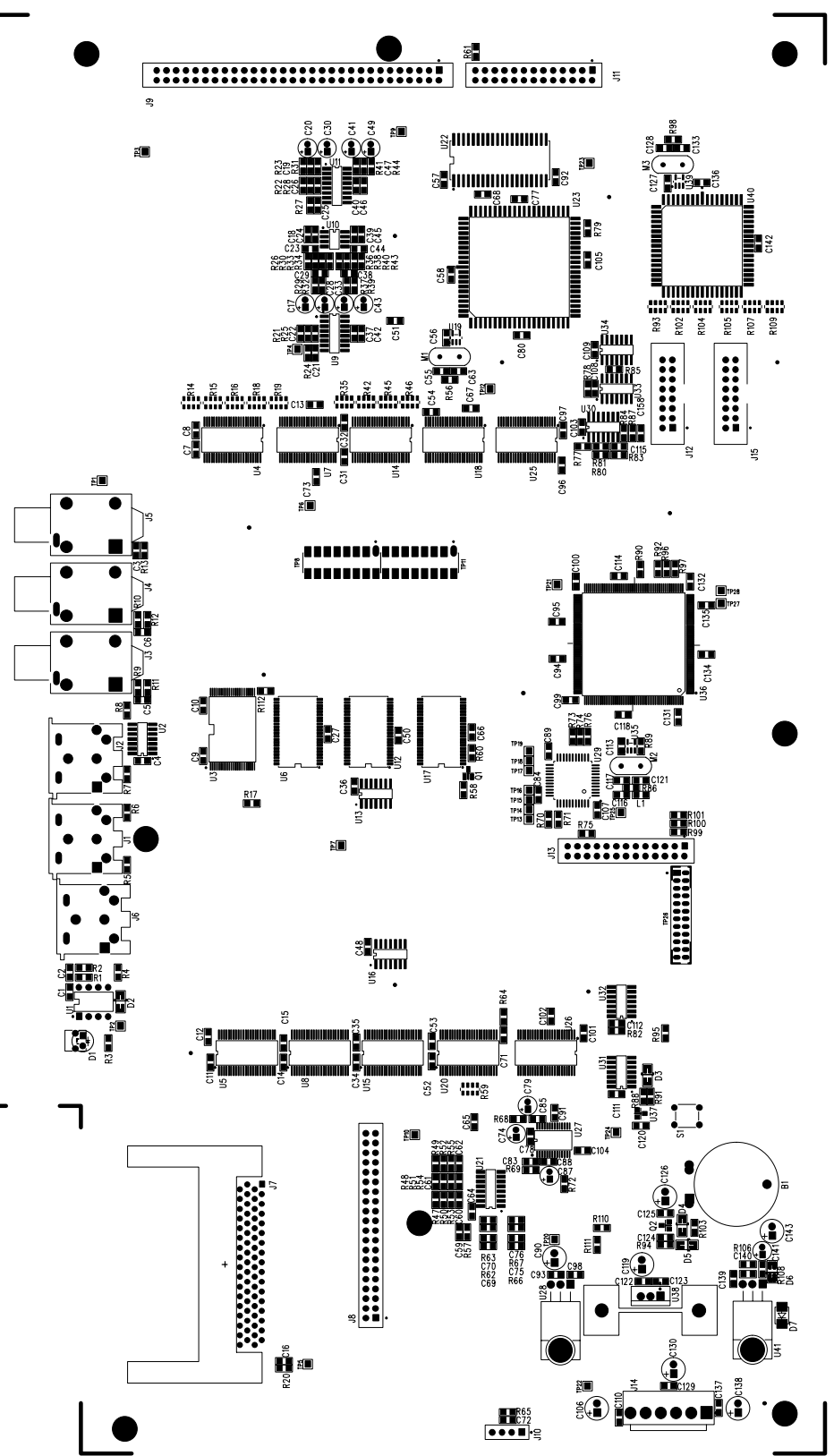
COMPANY: ALESIS
 TITLE: A6 MAIN PCB
 PART NUMBER: 9-40-0193-B
 ASSY NUMBER: 9-79-0193
 FILENAME: A6MN05A.SCH
 SCALE: SHEET 4 OF 4

TEST POINTS

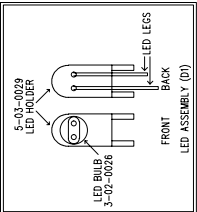
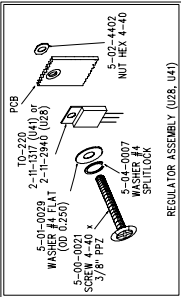
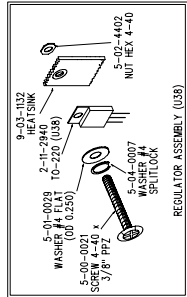
TP5	TP3	TP12	TP8	TP23	TP22	TP4	TP10
TP15	TP7	TP2	TP1	TP21	TP25	TP24	TP1
TP20	TP9	AD0					



ALESIS 9-40-0193-B A6 MAIN PCB ASSEMBLY DRAWING

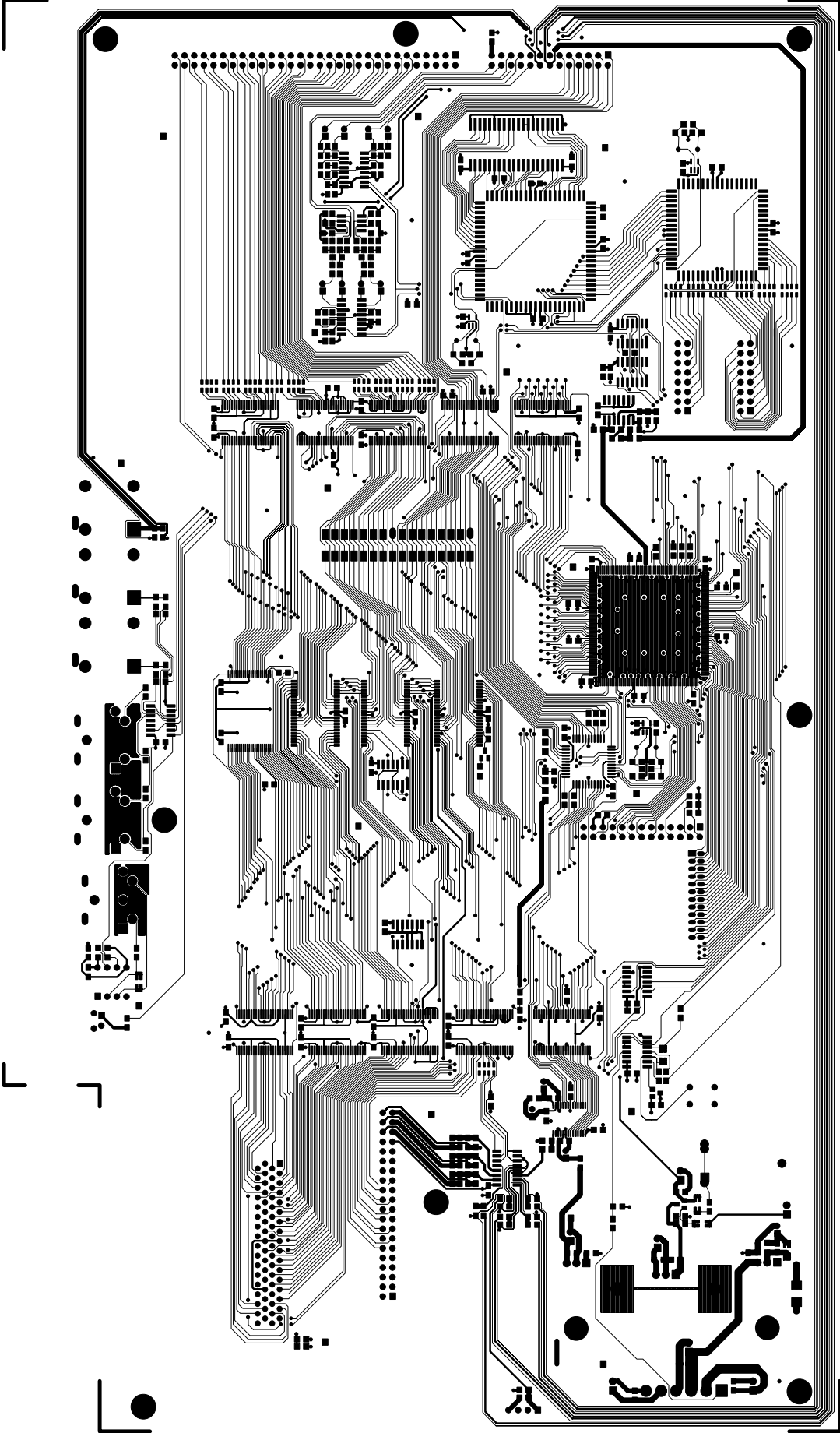


1. Tie all leads to external leads thru 60 mils (2.6mm).
2. Do not start on components on the bottom side (U14-U17) (1-56-0002).
3. Do not start on components on the bottom side (U14-U17) (1-56-0002).
4. Assemble DILLED (3-02-0026) and LED holder (5-03-0029) by completely inserting the LED through the oval, and then bending the leads perpendicular to the oval. (See drawing).
5. Trim legs (see PART 5 removed). Can also substitute a 3-pin and a 4-pin (4-15-0004) 0.1" unrounded SIL header.
6. Refer to drawing for the regulator assemblies (U28, U38, U41).



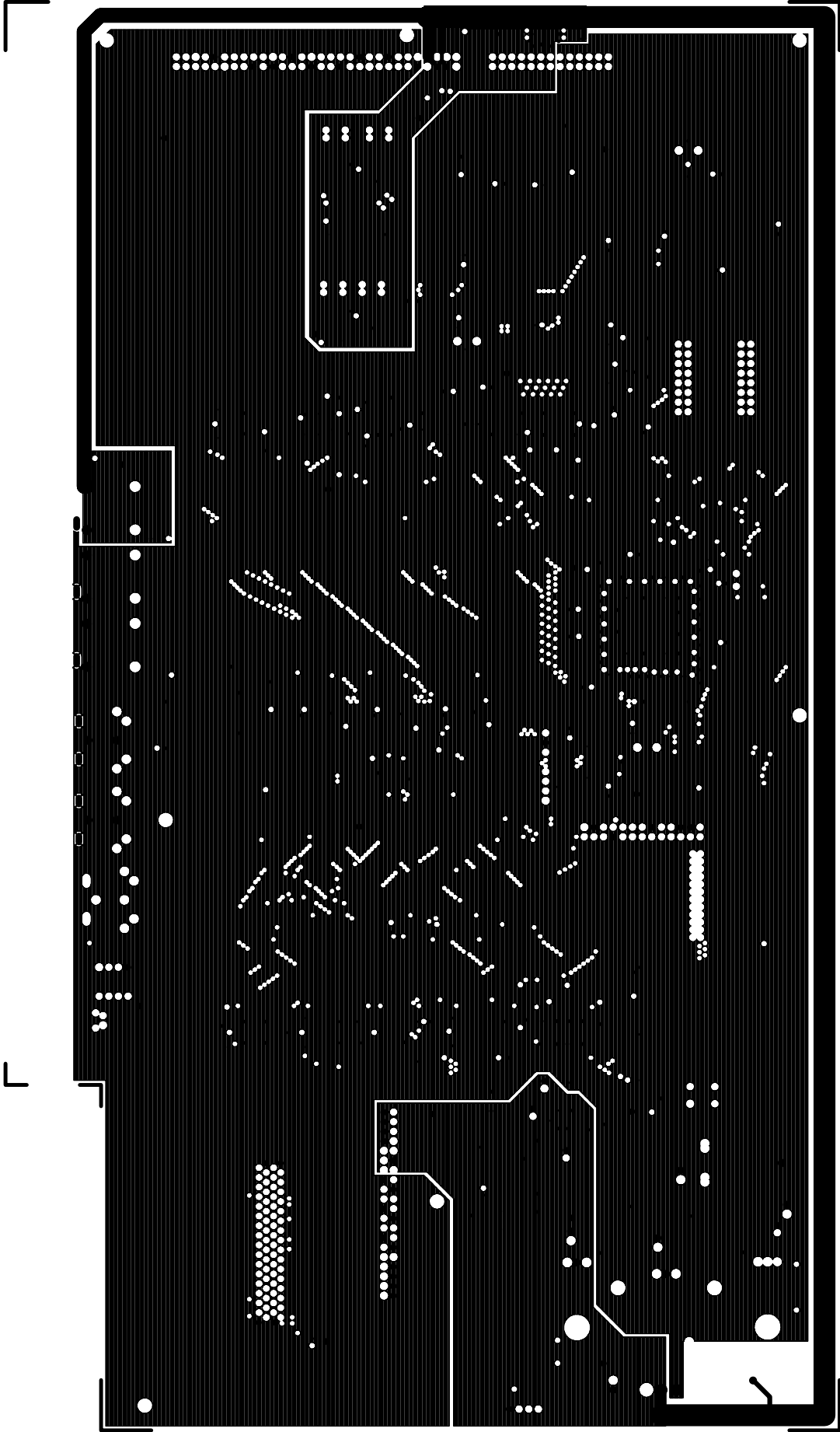
ALESIS 9-40-0193-B "TOPASSY"





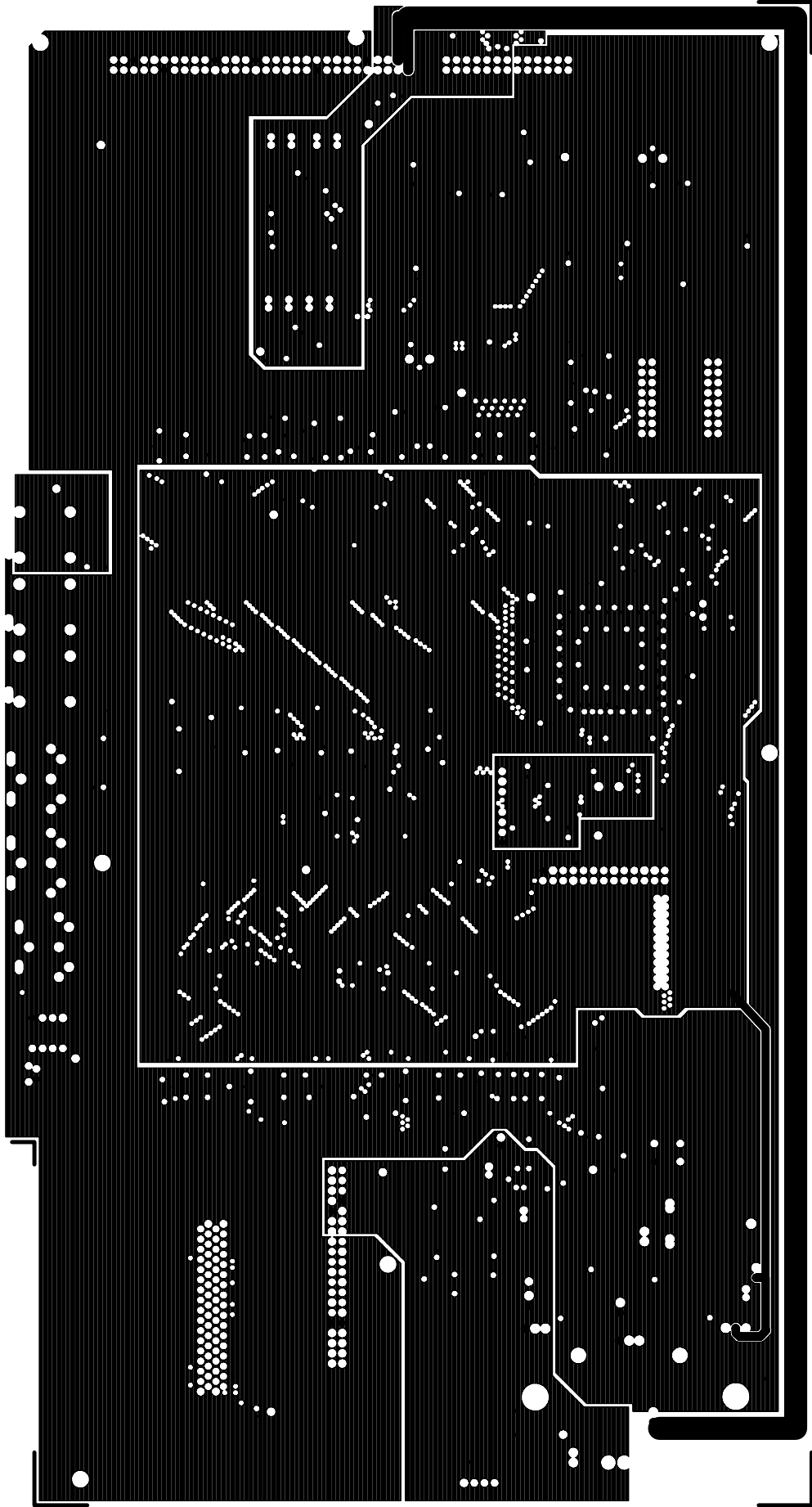
ALESIS 9-40-0193-B "TOP TRACE"





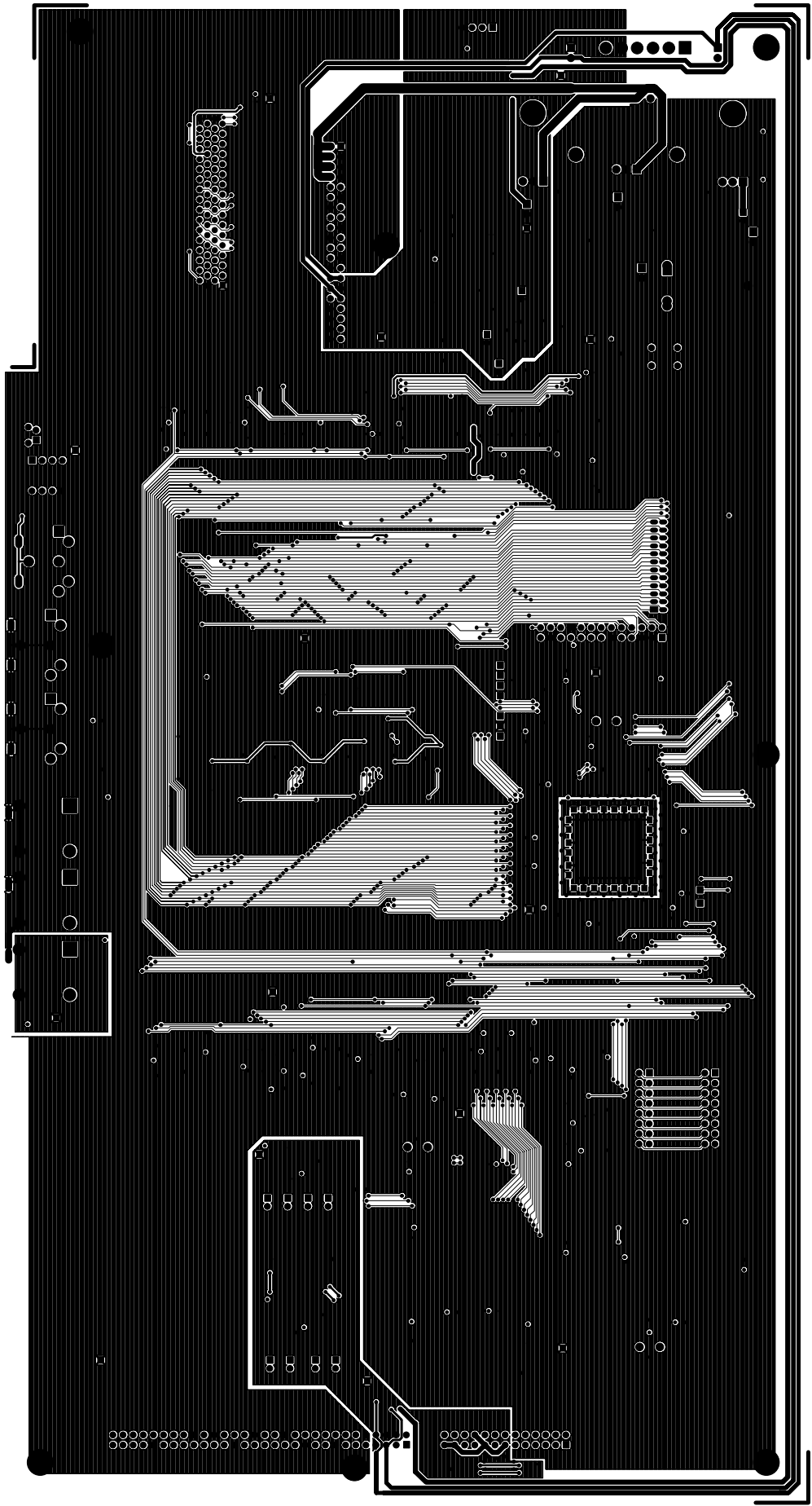
ALESIS 9-40-0193-B "GNDPLANE: LAYER 2"





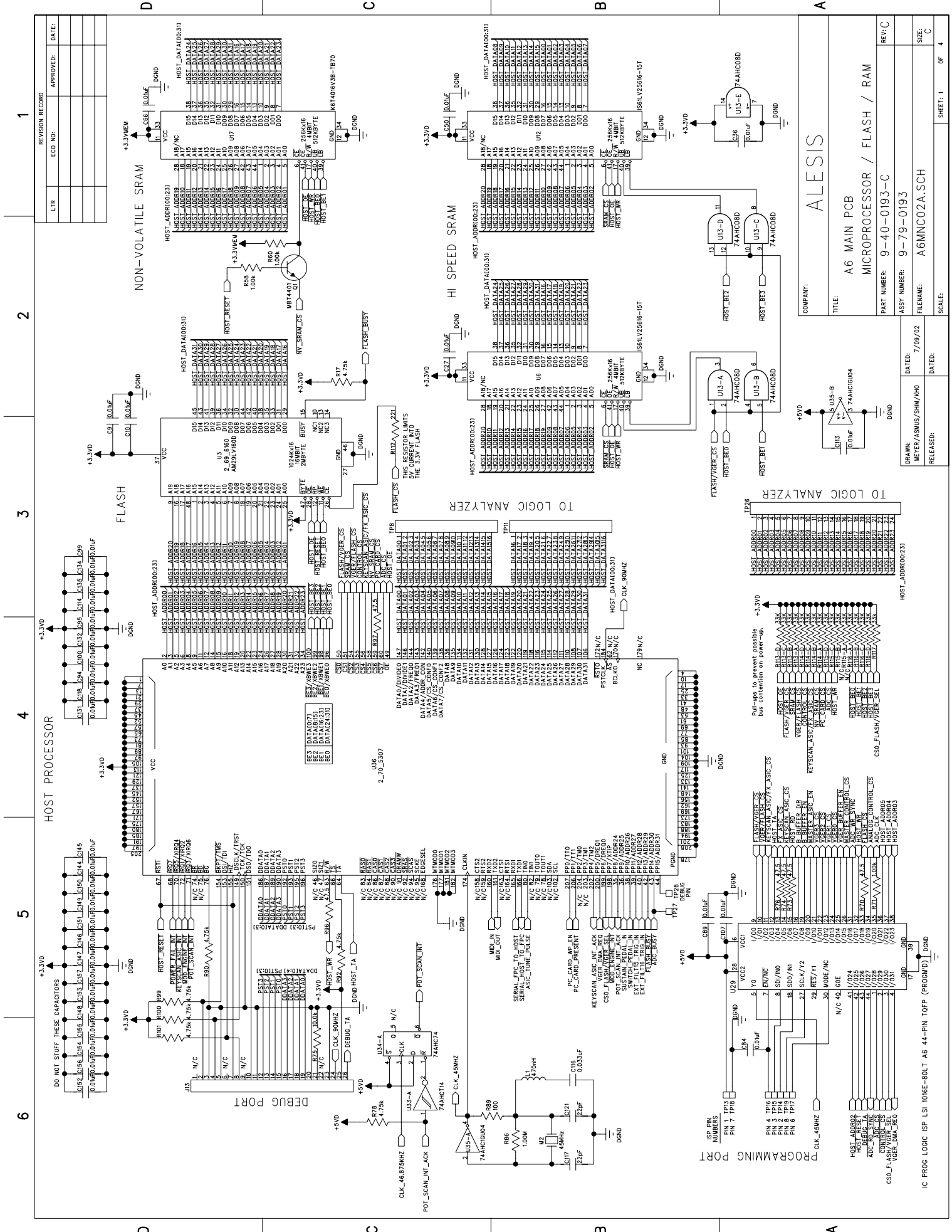
ALESIS 9-40-0193-B "PWRLANE: LAYER 3"





ALESIS 9-40-0193-B "BOTTRACE"





REVISION RECORD

LTR	ECO NO:	APPROVED:	DATE:

COMPANY: ALESIS

TITLE: A6 MAIN PCB

MICROPROCESSOR / FLASH / RAM

PART NUMBER: 9-40-0193-C

ASSY NUMBER: 9-79-0193

FILENAME: AGMNC02A.SCH

SCALE: SHEET: 1 OF 4

DRAWN: MFE/BE/ASMS/SHH/AHO

DATE: 7/09/02

RELEASED:

DATE:

IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)

IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)

IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)

IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)

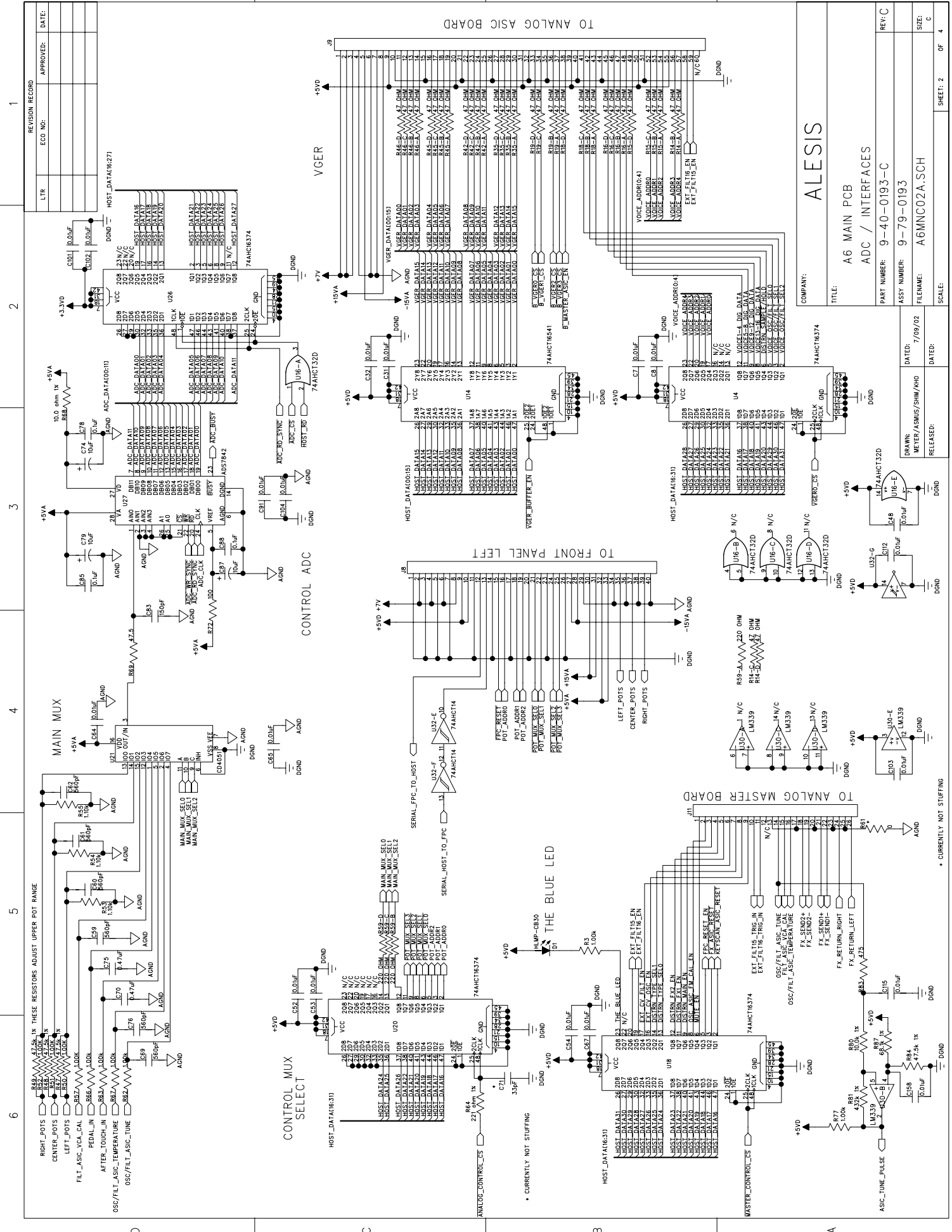
IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)

IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)

IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)

IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)

IC PROG LOGIC ISP LSI 1016E-80LT A6 44-PIN TQFP (PROGRAM)



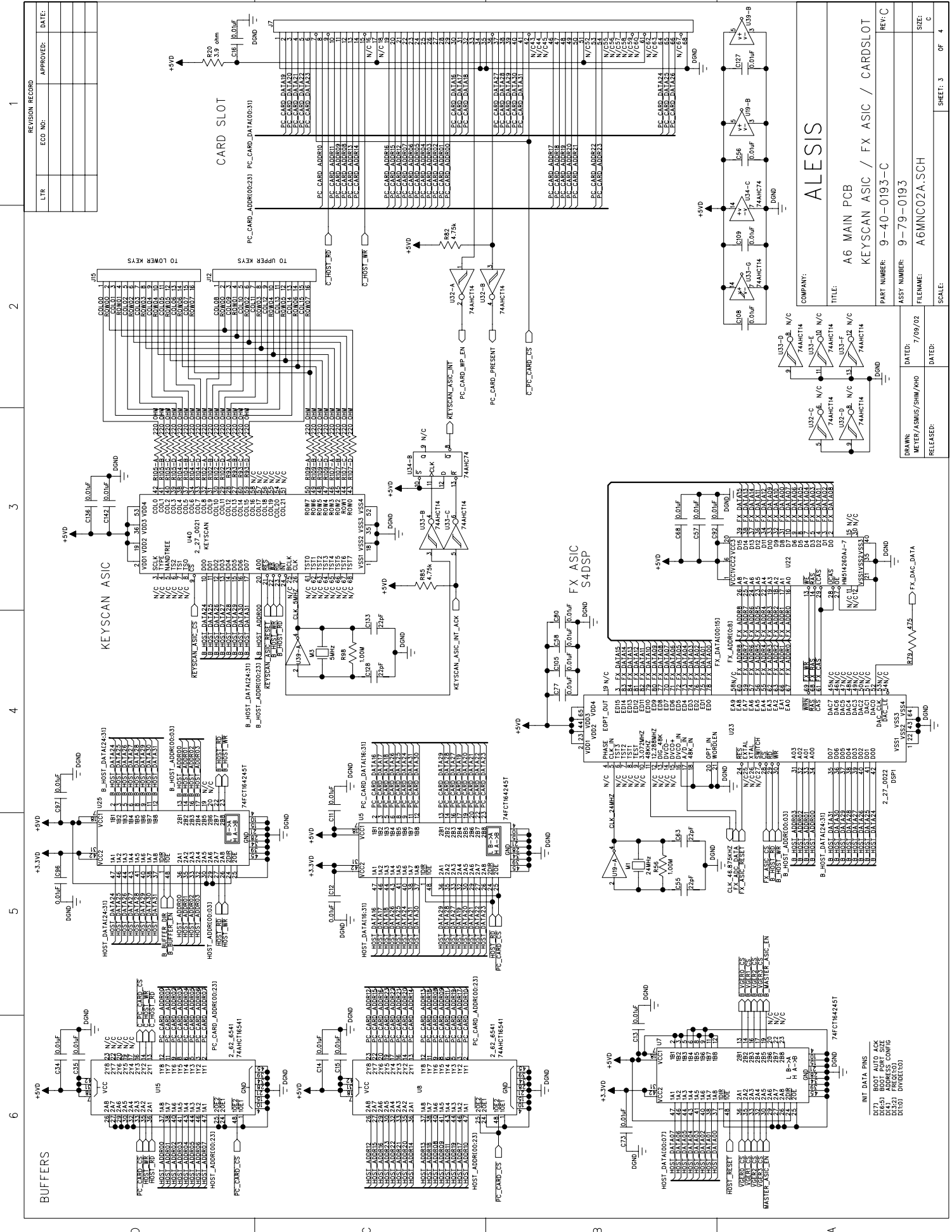
REVISION RECORD	APPROVED:	DATE:
LTR		
ECD NO:		

COMPANY:	ALESIS
TITLE:	A6 MAIN PCB
ADC / INTERFACES	
PART NUMBER:	9-40-0193-C
ASSY NUMBER:	9-79-0193
FILENAME:	AGMNC02A.SCH
SCALE:	

DATE:	7/09/02
DESIGNED BY:	MEYER/ASMUS/SHM/AHO
RELEASED:	

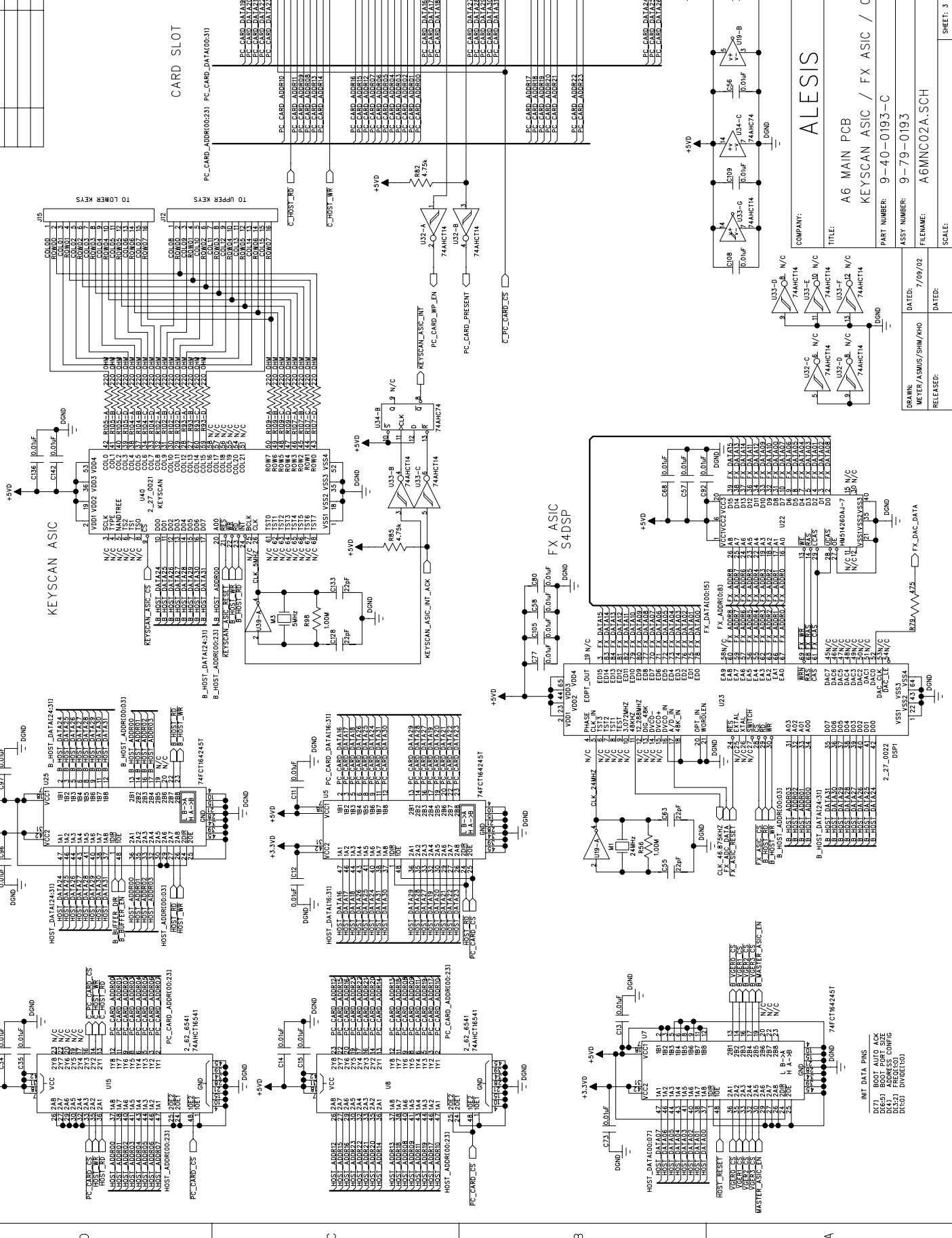
REV:	C
SIZE:	C
SHEET:	2
OF:	4

* CURRENTLY NOT STUFFING



1
2
3
4
5
6

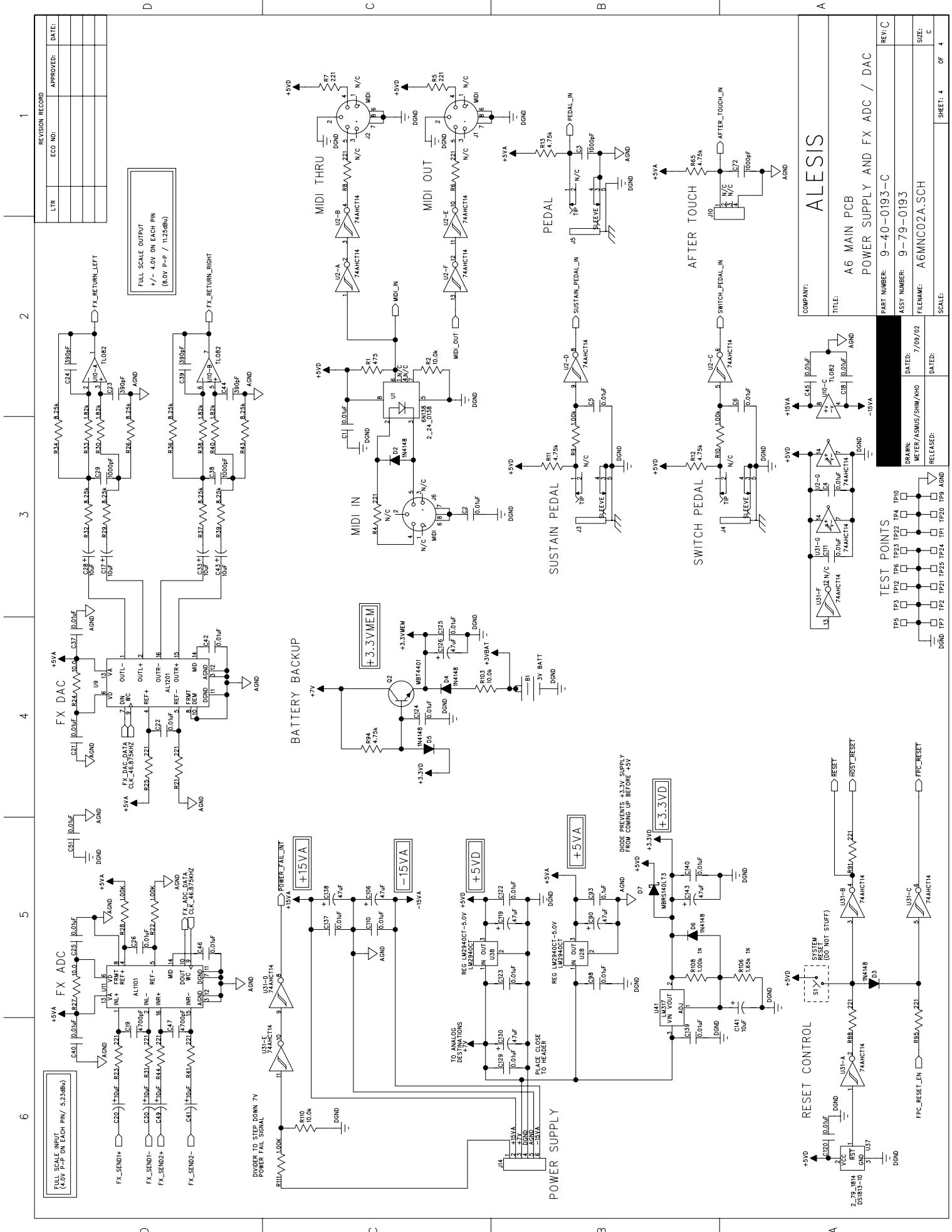
REVISION RECORD
LTR ECO NO: APPROVED: DATE:



COMPANY: ALESIS
TITLE: A6 MAIN PCB
KEYSCAN ASIC / FX ASIC / CARDSLOT
PART NUMBER: 9-40-0193-C
ASSY NUMBER: 9-79-0193
DRAWN: MEYER/ASM/S/SHM/AHO
RELEASED:
DATED: 7/09/02
DATE:

FILENAME: AGMNC02A.SCH
SCALE:
SHEET: 3 OF 4
SITE: C

INIT DATA PINS
D(7) BOOT_AUTO_ACK
D(6) BOOT_PORT_SIZE
D(5) CONFIG
D(4) FREQUENCY
D(3) DVIDE(10)

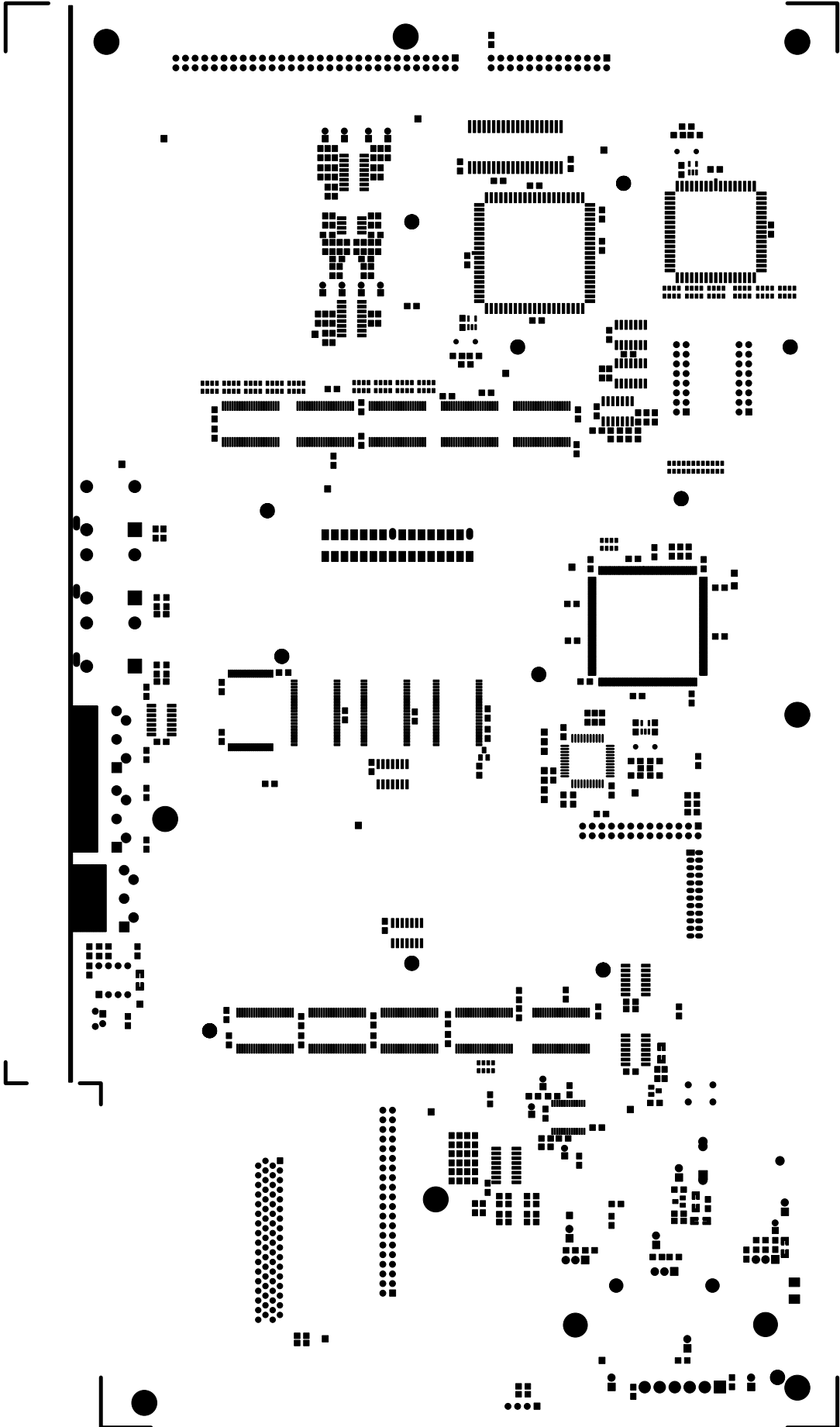


REVISION RECORD		DATE:
LTR	ECD NO:	APPROVED:

COMPANY:		ALESIS	
TITLE:		A6 MAIN PCB	
PART NUMBER:		POWER SUPPLY AND FX ADC / DAC	
ASSY NUMBER:		9-40-0193-C	
FILENAME:		AGMNC02A.SCH	
SCALE:			
DRAWN:		MAYEB/ASMIUS/SHM/AHO	
RELEASED:			
DATED:		7/09/02	

TEST POINTS	
TP1	TP2
TP3	TP4
TP5	TP6
TP7	TP8
TP9	TP10
TP11	TP12
TP13	TP14
TP15	TP16
TP17	TP18
TP19	TP20
TP21	TP22
TP23	TP24
TP25	TP26
TP27	TP28
TP29	TP30
TP31	TP32
TP33	TP34
TP35	TP36
TP37	TP38
TP39	TP40
TP41	TP42
TP43	TP44
TP45	TP46
TP47	TP48
TP49	TP50
TP51	TP52
TP53	TP54
TP55	TP56
TP57	TP58
TP59	TP60
TP61	TP62
TP63	TP64
TP65	TP66
TP67	TP68
TP69	TP70
TP71	TP72
TP73	TP74
TP75	TP76
TP77	TP78
TP79	TP80
TP81	TP82
TP83	TP84
TP85	TP86
TP87	TP88
TP89	TP90
TP91	TP92
TP93	TP94
TP95	TP96
TP97	TP98
TP99	TP100

1	2	3	4	5	6
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ALESIS 9-40-0193-C "TOPSMK"

